

UCC39421 3.3-V SEPIC Evaluation Board

Power Supply Control Products

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5 +1.8	List of Materials		5
0 0	C6 10 μF 10 V	3 L1A 3.76 µН @ 2.7 A dc	
0 0 0	VOUT V @ 1.0 A MAX $+ C7,C8 C9 C9 C1 C10 (OPTIONAL) 10 \mu F 10 V$ 6.7 8 1 - 2 C7 A dc 6.3 V 6.3 V 5 SI6562DQ (P) Q1B C10 = 2.7 A dc GPTIONAL) C10 = 2.7 A dc GPTIONAL = 2.7	C3 C3 C3 C3 C3 C3 C3 C3 C3 C3	$\begin{array}{c c} C1 \ 120 \ pF \\ \hline R4 \\ 33 \ k\Omega \\ 2200 \ pF \\ \hline 150 \ k\Omega \\ 1\% \\ \hline R3 \\ 40.2 \ k\Omega \\ 1\% \\ \hline R3 \\ 40.2 \ k\Omega \\ 1\% \\ \hline R3 \\ 40.2 \ k\Omega \\ 1\% \\ \hline R3 \\ 40.2 \ k\Omega \\ 1\% \\ \hline R3 \\ 40.2 \ k\Omega \\ 1\% \\ \hline R3 \\ \hline R5 \\ \hline \end{array}$
	+V _{IN} +V _{IN} C5 0.1 µF R8 PROV		1% S 1 MΩ O C11 120 pF SYNC/ PROV SHUTDOWN O UDG_9920

Contents

Figure 1. Evaluation Module Schematic

UDG-9920



1 Introduction

The UCC39421 SEPIC demo board implements a complete 330-kHz, 3.3-V SEPIC converter. The user needs only to supply an input voltage and a load. A list of materials, giving the component part numbers and case sizes, is given in Table 1. The schematic is shown in Figure 1 and a typical efficiency curve is shown in Figure 2.

2 Evaluation Board Features

- 330-kHz fixed frequency operation
- Synchronous rectification
- Current-mode control
- V_{IN} range of 1.8 V to 6.0 V
- V_{OUT} of 3.3 V at 1 A
- Output ripple < 50 mV peak-to-peak at 1-A load
- High efficiency of up to 90%
- PFM mode for improved efficiency at light load
- Synchronization/shutdown input

3 Operation

3.1 Input Voltage and Maximum Load

The converter operates with an input voltage between 1.8 Vdc and 6.0 Vdc. Once the converter is running, the input voltage can drop as low as 1.5 V at light load. The maximum allowed load is dependent upon the input voltage. At low input voltages, the dual MOSFET may get too hot, or peak current limit may be initiated. The load can be as high as 1-A steady state with an input of 2.5 V or greater. (Do not exceed an input voltage of 8.0 Vdc absolute maximum.)

Higher load currents can be supplied by using a larger MOSFET (with more heatsinking) and lowering the value of the current sense resistor (R10).

The stray inductance of the input power leads should be kept to a minimum to avoid input filter oscillation. If long leads are used, it is recommended that a $100-\mu$ F tantalum capacitor be added across the input terminals of the evaluation board. This lowers the Q of the input stage, and prevents potential loop oscillation.

3.2 PFM Mode

The UCC39421 is designed to automatically transition from fixed-frequency PWM operation to PFM (pulse frequency modulation) mode when the voltage on the COMP pin drops below the voltage programmed by the user on the PFM pin. This greatly improves efficiency at light load. With the component values supplied on the evaluation board, this transition occurs around a load current of 200 mA. The exact point will vary with input voltage. If desired, this feature can be disabled by grounding the PFM pin. (Note that if R3 is replaced by a jumper, the value of R2 must be increased by the value of R3 to maintain the same output voltage.)

3.3 Synchronization/Shutdown Input

Terminals are provided for connecting to the synchronization/shutdown input. This input may be left open (since pull-down R5 is included), in which case the converter runs freely at approximately 330 kHz. If desired, an external clock (0 V to 2 V peak minimum) may be applied to synchronize the PWM to a higher frequency. The duty cycle of the clock is not critical, but it must have a pulse width of at least 100 ns.

If the synchronization/shutdown input is held high (greater than 2 V) for over 20 μ s, the converter initiates shutdown.

3.4 Low Power Mode

The UCC39421 also has a low-power mode feature, designed to improve the efficiency at light to medium loads by reducing the gate drive voltage to the N channel. Normally the device selects the highest voltage available (usually VPUMP) to drive the gate of the ground-referenced FET. However, when the COMP voltage drops below 0.5 V, the device switches the FET gate drive to the lower voltage (VIN) to reduce losses. (Note that the drive level to the synchronous rectifier FET will always be VPUMP.) In some circumstances, if VIN is too low (such as below 2.5 V), this may be undesirable, even at light load. In these cases, low-power mode can be disabled by summing a small (20 mV) dc bias onto the voltage at the ISENSE pin. Provisional resistor R8 serves this purpose on the evaluation board. By installing a 270-k Ω resistor in place for R8, low-power mode is disabled. Note that low-power mode operates independently from PFM mode, and can be used in applications where PFM has been disabled.

3.5 Optional Schottky Diode

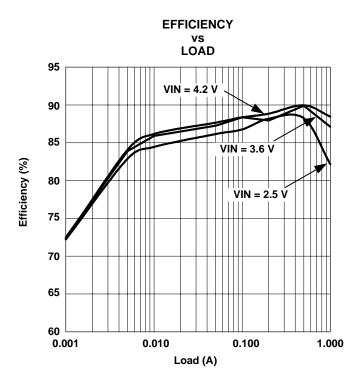
The evaluation board comes with a small Schottky diode installed in parallel with the synchronous rectifier. This optional diode improves efficiency by approximately 1%, by conducting the output current during the anti-cross-conduction delay times. During these times (about 35 ns at rectifier turn-on and turn-off), both MOSFETs are turned off. Without the diode installed, the output current must flow through the body diode of the rectifier MOSFET during these short intervals, thereby lowering efficiency.

3.6 Provisional Noise Filter Capacitors

The evaluation board comes with a provisional capacitor for added noise filtering (C11). This part is not installed, but can be used to filter the leading edge spike on the current-sense signal, supplementing the leading edge blanking built into the UCC39421.

For more application information, please consult the UCC39421 datasheet, TI Literature No. SLUS246.

4 Efficiency



5 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	SIZE
C1	120 pF ceramic capacitor			0805 chip
C2	2200 pF ceramic capacitor			0805 chip
C3, C5	0.1 µF ceramic capacitor			0805 chip
C4	1 μF ceramic capacitor			1206 chip
C6, C10	10 μF, 10 V, MLC capacitor	Taiyo Yuden	LMK325BJ106MN	1210 chip
C7, C8	100 μF, 6.3 V capacitor	Sanyo Poscap	6TPC100M	
C9	10 μF, 6.3 V, MLC capacitor	Taiyo Yuden	JMK316BJ106ML	1206 chip
C11 (provisional)	120 pF ceramic capacitor			0805 chip
D1 (optional)	1 A Schottky diode	Zetex	ZHCS1000	SOT-23
D2	0.2 A Schottky diode	Zetex	BAT54	SOT-23
L1	3.76 µH @ 2.7 A dc inductor	BH Electronics	511-0033	
Q1	Dual MOSFET (N/P)	Temic	Si6562DQ	TSSOP-8
R1	150 kΩ, 1%, 0.1 W metal film resistor			0805 chip
R2	49.9 k Ω , 1%, 0.1 W metal film resistor			0805 chip
R3	40.2 kΩ, 1%, 0.1 W metal film resistor			0805 chip
R4	33 kΩ, 5%, 0.1 W metal film resistor			0805 chip
R5	1M, 5%, 0.1 W metal film resistor			0805 chip
R6	2 kΩ, 5%, 0.1 W metal film resistor			0805 chip
R7	1 kΩ, 5%, 0.1 W metal film resistor			0805 chip
R8 (provisional)	Provisional resistor (not installed)			0805 chip
R9	150 kΩ, 1%, 0.1 W metal film resistor			0805 chip
R10	0.025 Ω, 5%, 0.5 W film resistor		LIRC LRC- RF1206-01-R025-J	1206 chip
U1	UCC39421PW			16-pin TSSOP

Table 1. Evaluation Board List of Materials



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